## REMARKS

Applicants reaffirm herein the election of the Group I claims (claims 1-10) for prosecution that was made without traverse on September 1, 2005. Claims 11-20 drawn to the non-elected distinct invention are canceled herein without prejudice to applicants' right to file a divisional application. Claims 1 and 3-10 remain pending in the application with the present amendments.

It is respectfully submitted that the replacement sheet containing amended FIGS. 1 and 2 now labeled "(PRIOR ART)" overcomes the prior drawing objection.

In the Office Action, claims 1-10 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,798,561 to Sato ("Sato"). In addition, claims 1-10 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,320,972 to Wylie ("Wylie"). For the reasons set forth below, applicants respectfully submit that the claims as amended herein overcome the rejections, and place the application in condition for allowance.

In the bipolar transistor according to embodiments of the invention, the collector pedestal is arranged so that it lies at a greater distance from the extrinsic base. This helps reduce capacitance between the collector and the extrinsic base. The way this is accomplished in the present invention is to reduce the area of an upper surface of the collector pedestal so that the intrinsic base overlies all of that area. In addition, a dielectric region is provided along a slanted sidewall of the collector pedestal. As now recited in

claim 1, the collector pedestal has an upper surface that is at least substantially planar.

The area of the upper surface is reduced, so that it is less than an area of a lower surface

of the collector pedestal. The reduced upper surface area of the collector pedestal is such

that the intrinsic base overlies all of the area of that upper surface area. A dielectric region

extends along a slanted sidewall of the collector pedestal (See dielectric region 170; FIG. 3

and dielectric 252; FIG. 16) between the upper surface and the lower surface and extends

along that sidewall adjacent to the upper surface of the collector pedestal.

Applicants submit that these features are neither taught nor suggested by

Sato or Wylie. As seen in FIG. 1 of Sato, intrinsic base 1019 clearly does not overlie all of

the area of the collector pedestal 1003. In addition, Wylie neither teaches nor suggests the

structure recited in claim 1. Wylie neither teaches nor suggests a dielectric region

extending along a slanted sidewall of a collector pedestal adjacent to its upper surface.

Wylie merely shows oxide regions 40 (FIG. 8) placed relatively far from the collector

pedestal 54. The oxide regions 40 do not extend along a slanted sidewall of the collector

pedestal adjacent to an upper surface, for which all of the area underlies an intrinsic base.

Support for the present amendments is provided, *inter alia*, at paragraphs

[0033], [0034] and [0045] and in the drawings including FIGS. 3, 10 and 16.

Serial No. 10/708,340 Hiroyuki Akatsu et al.

This response is filed with a petition to extend the period for response to the Office Communication by one month. If any other fee is due in connection with this response, please debit the Deposit Account No. 09-0458 of the Assignee International Business Machines Corporation. If there is an overpayment, please credit the same account.

Respectfully submitted,

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